An InP/InGaAs SHBT Technology for High-Speed Monolithic Optical Receivers

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Abstract

In this paper we present a manufacturable InP/InGaAs SHBT technology suitable for monolithic integration of high-data-rate optical receivers. We investigated the fabricated SHBT and found that they are essentially insensitive to processing variations. The satisfactory device yield and uniform device performance in a research laboratory environment suggested the robustness of InP-based SHBT technology. Our device and circuit results augment the feasibility of InP HBT for both optoelectronic and microelectronic applications.

INTRODUCTION

Despite the economy downturn and the delay in the deployment of high-data-rate optical link systems, the continuing evolution of optoelectronic industry toward higher data-rate remains a strong incentive for device technology development of next-generation ultra-fast optoelectronic components. Indium phosphide HBT have gained its presence in 40Gb/s OEICs over the past few years and are still the most viable technology for optoelectronic front-end circuits in >40Gb/s arena. Continuing development of InP SHBT technology shows that this material system can yield the highest device speed among their competing technologies such as SiGe technologies while maintaining reasonable device DC characteristics [1]. The capabilities of monolithic integration of photodetectors in InP HBT technology also offer favorable cost and manufacturability advantages over other hybrid solutions such as SiGe in high-speed optical receivers.

In this paper, we will present an InP-based carbon-doped-base SHBT technology that has the potential for manufacturable InP-based circuits. This lab-based device technology, despite the lack of well-controlled mass-production environment, shows uniform device/circuit characteristics and potential manufacturability. Our results indicate that the InP-based HBT technology has inherently robust device characteristics and low processing-related susceptibility. With the availability of large-dimensional InP substrates, InP SHBT technology will be still suitable for high performance RF electronics and optoelectronic circuits at a lower material cost.

FABRICATION PROCESSES AND DEVICE PERFORMANCE

The fabrication processes are developed on 2-inch InP substrates using contact photolithography techniques. The baseline SHBT processing has an emitter of 15 μm^2 with a stripe width of 3 μm. The detailed device processing steps and device CAD layout optimization were presented in [2]. A schematic cross-sectional drawing of the constituent device components in a monolithic optical receiver is shown in Fig. 1. In addition to device-level processing, two metal interconnection layers are used in the circuit fabrication. MIM capacitors are formed by a dielectric layer inserted in between Metal-1 and Metal-2 layers. NiCr films and semiconductor layers are used as resistors in circuit fabrications.

Two sets of fabrication processes are established to address different needs in high-speed optical link applications. For 40Gb/s SR OEICs, the HBT has a f_T of 124 GHz and f_{max} > 220 GHz (Process I). The integrated PIN has a responsivity of 0.35 A/W at 1550nm wavelength and 44 GHz bandwidth. For VSR applications, the HBT has a f_T of 170 GHz and f_{max} > 220 GHz and the responsivity of the integrated PIN is 0.18 A/W (Process II). Typical RF performances of the HBTs are shown in Fig. 2.

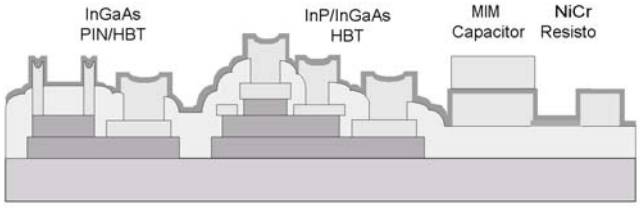


Fig. 1 A schematic drawing of monolithically integrated PIN+HBT technology

DEVICE UNIFORMITY

In the study of device uniformity, reference SHBT devices were generated at the PCM region of each reticle. They are then uniformly distributed across a wafer. The DC and RF characteristics of fabricated devices are measured using an HP4145 and an HP8510C network analyzer.

Typical device yield is >99% on a 2-inch wafer. A large-signal symbolically defined device model was developed using an RF-parameter optimization scheme. The resulting device modeling accurately simulates both DC and RF device characteristics. Extracted parameters are used to study the source of variation in fabrication processes and also to facilitate circuit design.

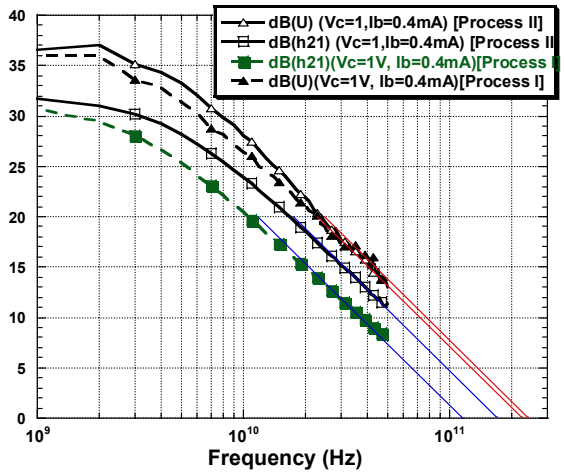


Fig. 2. Typical f_T and f_{max} plots for InP SHBTs with different collector thicknesses. solid lines: Process I; dashed lines: Process II.

Fig. 3 shows typical histograms of the measured current gain, f_T, emitter resistance, collector resistance, and base ideality factor across a 2-inch InP wafer. The measurement results are summarized in Table.1. The current gain is measured at V_{BE} = 0.9V and f_T is extrapolated from dB(h21) with a slope of 20 dB/decade at V_{ce} = 1.0V and I_b= 0.4 mA. The resistances as well as base ideality factor are extracted from an S-parameter measurement under saturation modes

The average current gain is 36.2 with a standard deviation of less than 2%. The average f_T is 124.6 GHz with a variation of 1.1 %. The measured current gain and f_T's show little variation across a wafer and are reproducible between processing batch runs. In the study of processing-induced variations, the measured and extracted device parameters of interest are resistances at each terminal, i.e., emitter, base, and collector. The extracted resistances approximately account for the sum of metal contact resistance and the via-hole access resistances. The control of emitter resistance is of crucial importantance because it can drastically affect the current gain and high frequency performance. Another monitoring parameter is the base ideality factor. The base current ideality factor reveals information on wet-etching processing steps.

The base ideality factor shows an average of 1.39 with variation of ~ 1%, indicating the wet-etching steps are well-controlled. The emitter and base resistance, however, shows a wider variation. The source of variation is believed to be mainly from the via-hole RIE etching. Larger via-hole openings show less variation in the access resistance. Nevertheless, it is interesting to see that the resistance variation has little influence on the uniformity of the device performance for wide emitter devices. This result indicates that HBT devices can essentially be made insensitive to the variation in the resistances if the extrinsic resistances are optimized.

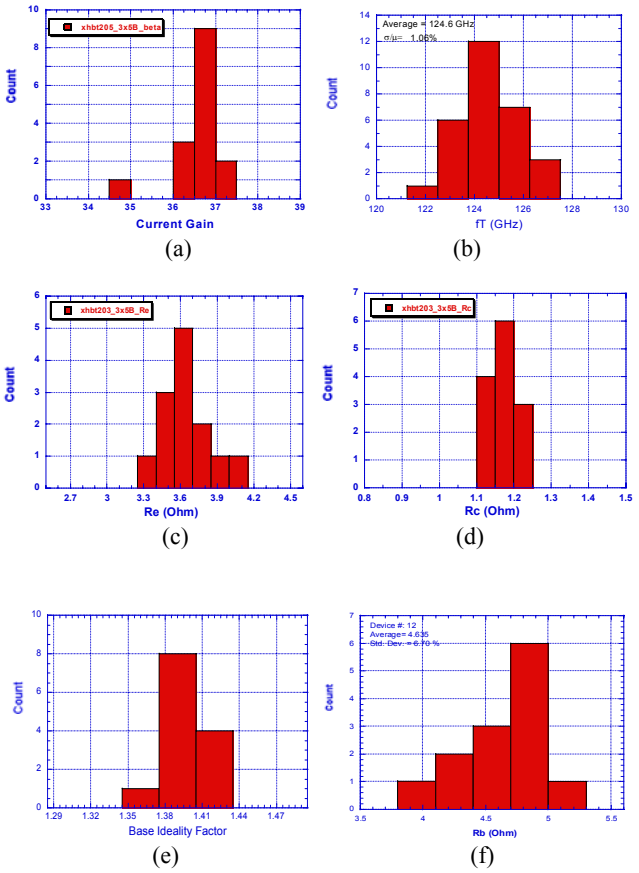


Fig.3 Histograms of measured (a) current gain, (b) f_T, (c) emitter resistance, (d) collector resistance, (e) base ideality factor, and (f) extracted base resistance

	β	f_T (GHz)	η_b	Re (Ω)	Rc (Ω)	Rb (Ω)
Average	36.2	124.6	1.395	3.65	1.16	4.64
Std (%)	1.7	1.1	1.05	6.1	3.3	6.7

Table 1. A summary of measured and extracted parameters

The reliability testing of the device is underway. Our preliminary result shows a current gain change of less than 10% with a 100 kA/cm^2 current stress at 150^{o}C after 1000 hours. More comprehensive reliability testing will be needed to come to a conclusion on the device reliability.

CIRCUIT PERFORMANCE

Several circuits have been fabricated using the InP SHBT technology described in this paper. They include single-ended TIA, differential-output TIA, single-ended PIN+TIA, and differential output PIN+TIA. Fig. 4 and 5 showed the photograph and performance of fabricated 40Gb/s single-ended PIN+TIA circuits. The circuit has a typical transimpedance gain of 200Ω and bandwidth of 33GHz at 25C operating at negative supply voltage of 3.4V. The mzximum output voltage swing is $0.5V_{p-p}$ and the return loss is greater than 12dB at 50GHz. Also shown in Fig. 6 and 7 are a photograph of a 40Gb/s differential PIN+TIA and the measured performance of a 40Gb/s differential TIA, respectively. The TIA has a transimpedance of 280 Ω with a bandwidth of > 40GHz. The return loss is less than 12 dB at 50 GHz and the group delay is less than 5 ps from 1-26GHz. The detailed circuit design and circuit performance of the differential PIN+TIA was presented in [3].

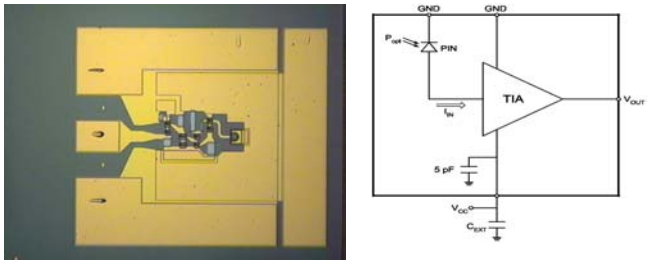


Fig. 4 Fabricated 40Gb/s single-ended PIN+TIA (XM-4001SE)and its circuit schematic diagram.

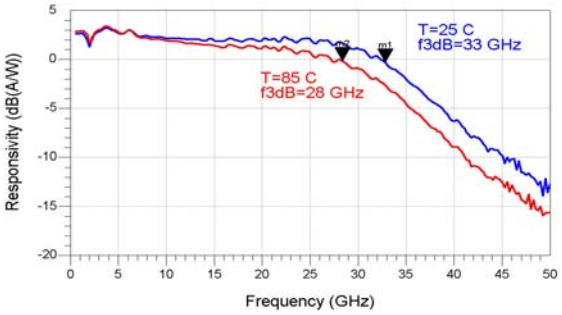


Fig. 5 Measured optical-to-electrical of 40Gb/s single-ended PIN+TIA.

The circuit yield and uniformity is compounded by the number of devices in a circuit, passive component uniformity, and compliance of design rules. Typical yield of the differential PIN+TIA circuit is 60 - 80%. Shown in Fig. 8 are histograms of bandwidth and transimpedance of the measured differential-output PIN+TIA. The average 3dB bandwidth of fabricated circuits is 40.9 GHz with a standard deviation of 6.3%. The average transimpedance is 199.3 Ω with a standard deviation of 9.9% across a 2-inch wafer. Excluding bad data points that were taken at the edge of the wafer, the result suggests high circuit uniformity. We attribute the variation in circuit performance mainly to the variation in the NiCr resistor across a wafer. A slight change in the resistor value at the output of the circuit results in considerable variations in the transimpedance gain and the circuit bandwidth.

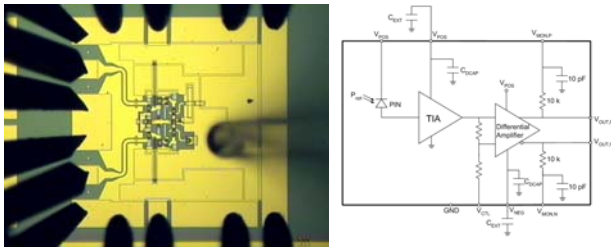


Fig. 6 Fabricated 40Gb/s differentil-output PIN+TIA (XM-4001DF)and its circuit schematic diagram.

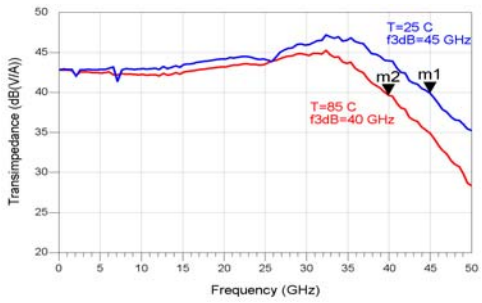
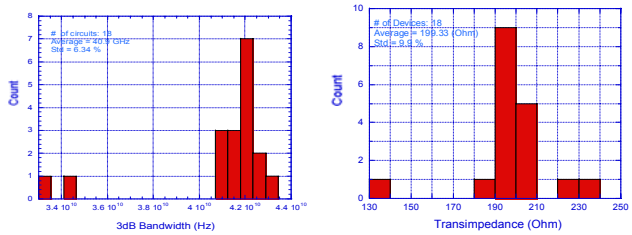


Fig. 7 Measured electrical-to-electrical of 40Gb/s differential-output TIA.



(a) (b)

Fig. 8 Histograms of (a) bandwidth and (b) transimpedance of 40Gb/s differential-output PIN+TIAs on a 2-inch wafer

CONCLUSIONS

In conclusion, we developed an InP/InGaAs SHBT technology that is suitable for future 40Gb/s monolithic OEIC receivers. We investigated the fabricated SHBT and found that they are essentially insensitive to processing variations. The satisfactory device yield and uniform device performance in a research laboratory environment suggested

the potential robustness of InP-based HBT. The fabricated OEIC circuits demonstrated the feasibility of InP SHBTs in high-speed optical receiver applications. Our results augment the feasibility of InP HBT for both optoelectronic and electronic applications.

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ACRONYMS

SHBT: Single Hetero-junction Bipolar Transistor
MIM: Metal-insulator-metal
RIE: Reactive ion etching
PCM: Processing control monitoring
TIA: Transimpedance Amplifier
PIN: p-intrinsic-n diode
OEIC: Optoelectronic Integrated Circuits
SR: short-reach
VSR: Very-short-reach

