

# Polyimide Passivated AlGaN–GaN HFETs With 7.65 W/mm at 18 GHz

Mark D. Hampson, Shyh-Chiang Shen, Randal S. Schwindt, R. Kirk Price, Uttiya Chowdhury, Michael M. Wong, Ting Gang Zhu, Dongwon Yoo, Russell D. Dupuis, *Fellow, IEEE*, and Milton Feng, *Fellow, IEEE*

**Abstract**—Current metal–organic chemical vapor deposition-grown AlGaN–GaN heterojunction field-effect transistor devices suffer from threading dislocations and surface states that form traps, degrading RF performance. A passivation scheme utilizing a polyimide film as the passivating layer was developed to reduce the number of surface states and minimize RF dispersion. Continuous-wave power measurements were taken at 18 GHz on two-finger 0.23- $\mu\text{m}$  devices with  $2 \times 75 \mu\text{m}$  total gate width before and after passivation yielding an increase from 2.14 W/mm to 4.02 W/mm in power density, and 12.5% to 24.47% in power added efficiency. Additionally, a  $2 \times 25 \mu\text{m}$  device yielded a peak power density of 7.65 W/mm at 18 GHz. This data suggests that polyimide can be an effective passivation film for reducing surface states.

**Index Terms**—Delta doping, Gallium nitride, heterojunction field-effect transistor (HFET), high-electron mobility transistor (HEMT), polyimide.

## I. INTRODUCTION

THE AlGaN–GaN heterojunction field-effect transistor (HFET) have shown much promise for their suitability as high-power electronic devices, and are improving rapidly with development. Prof. Eastman's group from Cornell University, Ithaca, NY, holds the current record for power density at 11.7 W/mm for their 100- $\mu\text{m}$  gate width device measured at 10 GHz [1], [2]. Furthermore, Nippon Electronic Corporation reported a 10-W/mm power density for a 1-mm device with a field-modulating gate at 2 GHz [3]. AlGaN–GaN HFETs have also been demonstrated at the circuit level; Cree reported a hybrid amplifier that delivered 102 W with a power density of 4.3 W/mm [4]. Despite these advances, difficulties remain in reliability and reproducibility.

An important problem that must be overcome before reaching the full potential of this technology is the dispersion effect, which is attributed to surface electron traps. Surface passivation using SiN decreases the number of surface states, increasing device performance [5]. However, disadvantages of using SiN for passivation are the stress induced by the film and the possibility of plasma damage from the plasma-enhanced chemical vapor deposition. This letter presents the use of polyimide passiva-

Manuscript received January 8, 2004; revised February 23, 2004. This work was supported in part by the National Aeronautics and Space Administration under Contract NAG3-2633, and in part by the Defense Advanced Research Projects Agency under Navy Grant N00014-95-1-1302. The review of this letter was arranged by Editor D. Ritter.

M. D. Hampson, S.-C. Shen, R. S. Schwindt, R. K. Price, and M. Feng are with the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA.

U. Chowdhury, M. M. Wong, T. G. Zhu, D. Yoo, and R. D. Dupuis are with the Microelectronics Research Center, The University of Texas at Austin, Austin, TX 78758 USA.

Digital Object Identifier 10.1109/LED.2004.826565

25 nm Al <sub>0.2</sub> Ga <sub>0.8</sub> N
Si Delta Doping
5 nm Al <sub>0.2</sub> Ga <sub>0.8</sub> N
1 nm AlN
2 $\mu\text{m}$ GaN
200 nm AlN
SiC Substrate

Fig. 1. Delta-doped binary barrier device layer structure of this work.

tion for AlGaN–GaN HFETs as an alternative method giving a low stress and low damage solution, effectively reducing the number of surface trapping states and the dispersion effect. We address the performance of the polyimide-passivated surfaces and demonstrate that it improves power density, gain, and power added efficiency (PAE).

## II. GaN HFET GROWTH AND PROCESSING

The Al<sub>x</sub>Ga<sub>1-x</sub>N–GaN ( $x \sim 0.2$ ) HFETs were grown by low-pressure metal–organic chemical vapor deposition (MOCVD) [6]. The growth process begins with a high-temperature ( $\sim 1070 \text{ }^\circ\text{C}$ ) AlN buffer layer of 100 nm thickness. The subsequent device layers are grown at  $\sim 1050 \text{ }^\circ\text{C}$ , beginning with 3  $\mu\text{m}$  of undoped GaN. On top of this is a 1-nm AlN barrier layer, followed by 30-nm layer of Al<sub>x</sub>Ga<sub>1-x</sub>N ( $x \sim 0.2$ ). The Si-delta doping occurs after 5 nm of growth of this last layer. The layer structure is shown in Fig. 1.

We achieved device isolation using a chlorine-based dry etching process using an inductively coupled plasma-reactive ion etching. Ohmic metal was deposited using optical lithography in a four-layer metal stack consisting of Ti–Al–Ni–Au. The samples were then alloyed at 870  $^\circ\text{C}$  for 30 s to minimize contact resistance. The gate pattern was created using e-beam lithography followed by a Ni–Au evaporation to form the Schottky gates. A layer of Ti–Au was then evaporated onto the sample to create probe pads and provide a good RF path. Finally, we spun on a 4:1 polyimide to thinner mixture and cured at 300  $^\circ\text{C}$  to ensure a low-stress film for surface passivation. Low film stress is important for GaN HEMTs because it reduces the change in threshold voltage after passivation, thereby reducing one factor that contributes to variations in threshold voltage across a chip. Typical film stresses for polyimide are less than 70 MPa, and are highly dependent on the type of polyimide deposited and the curing schedule [7], [8]. SiN film stress ranges from 300 to 2000 MPa depending on the deposition method [9]. This is the first reported time polyimide has been used to passivate AlGaN–GaN HFETs.

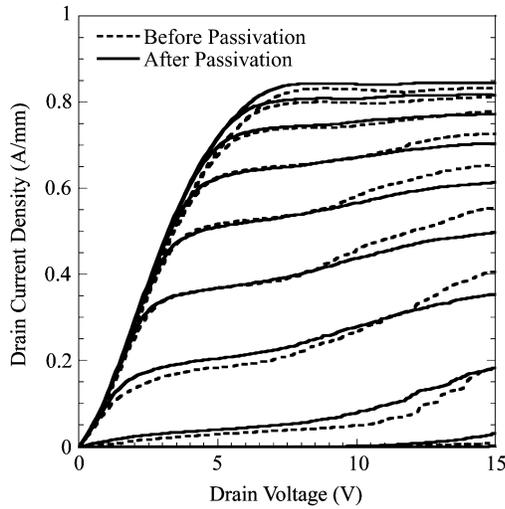


Fig. 2. Measured current-voltage curves in 1 V steps before and after passivation for a  $2 \times 75 \mu\text{m}$  device with a maximum  $V_{gs} = 1 \text{ V}$ .

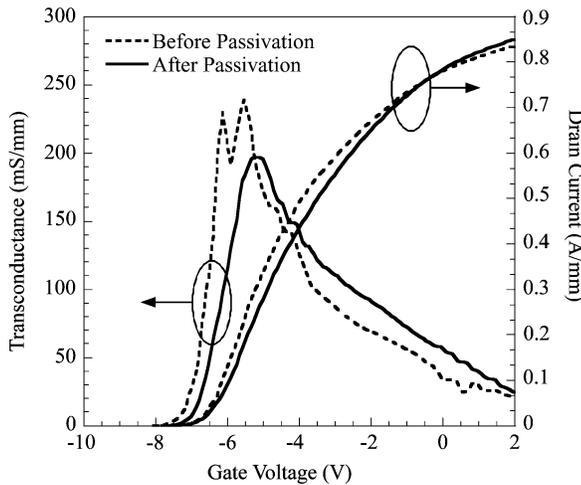


Fig. 3. Measured transfer characteristics before and after passivation for a  $2 \times 75\text{-}\mu\text{m}$  device at  $V_{ds} = 11 \text{ V}$ .

### III. RF RESULTS AND DISCUSSION

Before and after passivation we measured dc, RF, and passive load-pull characteristics for devices with two-finger  $0.23\text{-}\mu\text{m}$  gates with  $150\text{-}\mu\text{m}$  total gate peripheries. Load-pull characteristics were also measured for a two-finger  $0.23\text{-}\mu\text{m}$  gate device with a  $50\text{-}\mu\text{m}$  periphery after passivation.

The dc characteristics of a  $150\text{-}\mu\text{m}$  width device were measured using an HP4142 source/monitor unit and coplanar probes and are shown in Figs. 2 and 3. The drain current pinches off at  $V_{gs} = -7.5 \text{ V}$  and  $-7 \text{ V}$  before and after passivation, respectively. At  $V_{ds} = 11 \text{ V}$ , the peak transconductance was measured to be 240 and 200 mS/mm before and after passivation. The maximum drain current density was measured at  $V_{gs} = 2 \text{ V}$  and was 0.84 A/mm before passivation and 0.86 A/mm after.

High-frequency  $S$ -parameters were measured using an HP 8510C network analyzer and off-wafer calibration. Cutoff frequencies of 63 and 57 GHz were measured before and after passivation, respectively; this decrease is to be expected from the increased capacitance due to the polyimide layer.

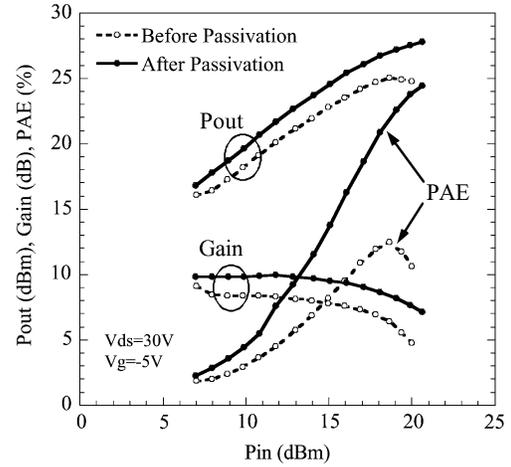


Fig. 4. Large-signal characteristics measured at 18 GHz of two different  $2 \times 150 \mu\text{m}$  devices on the same wafer with  $L_g = 0.23 \mu\text{m}$  before and after passivation.

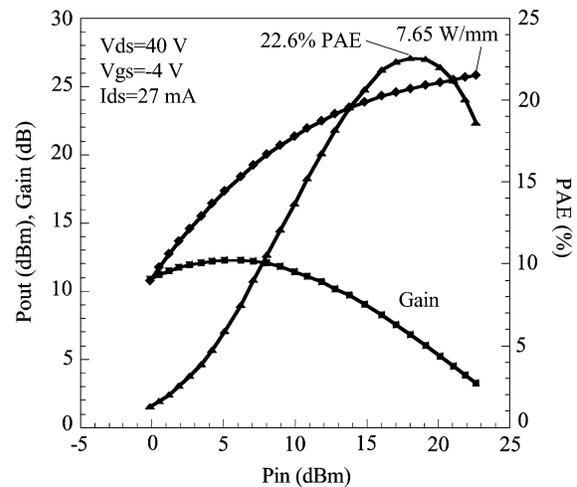


Fig. 5. Large-signal characteristics measured at 18 GHz of a  $2 \times 50\text{-}\mu\text{m}$  device with  $L_g = 0.23 \mu\text{m}$  after passivation.

A passive load-pull measurement setup was used to measure the large signal characteristics of several devices before and after passivation at 18 GHz; results representative of the wafer are shown in Fig. 4. The figure shows results from one device measured before passivation and a nearby device measured after passivation. In both cases, the devices were biased with 30 V on the drain and  $-5 \text{ V}$  on the gate. Each device had  $0.23\text{-}\mu\text{m}$  gates with  $150\text{-}\mu\text{m}$  total gate periphery. Before passivation, a peak output power of 25.07 dBm, or 2.14 W/mm power density, a peak PAE of 12.5%, and a maximum gain of 8.49 dB were measured. Polyimide passivation improved the peak output power to 27.8 dBm, 4.02 W/mm power density, 24.47% PAE, and 9.86 dB gain, suggesting that surface states were significantly reduced.

Load-pull measurements were also taken from a  $2 \times 25 \mu\text{m}$  gate width device, as shown in Fig. 5. The drain was biased at 40 V and the gate at  $-4 \text{ V}$ , giving 27-mA drain current. At 18 GHz a maximum power density of 7.65 W/mm was measured, with a peak PAE of 22.58%, and associated gain 6.81 dB. The heavy gain compression is attributed to leakage current in the buffer layer at high drain bias and device self-heating, both of which reduce the signal swing. The measured power density

for this device is the highest reported to date at 18 GHz. Other devices of the same size averaged 6.2 W/mm and 23% PAE at the same bias. The  $2 \times 25\text{-}\mu\text{m}$  gate width devices are expected to have higher power densities than larger area devices because there is less total heat and reduced signal attenuation down the width of the gate.

#### IV. CONCLUSION

We grew a unique AlGaIn–GaIn HFET layer structure with a binary barrier and delta-doping on a 4H-SiC substrate. The devices fabricated on this layer structure demonstrated significant improvement in output power density and PAE after a polyimide passivation process, which has never been attempted on AlGaIn–GaIn. The power density improved from 2.14 to 4.02 W/mm and the PAE increased from 12.5% to 24.47%, providing evidence that the polyimide reduced the number of surface states. A device with a  $2 \times 25\text{-}\mu\text{m}$  gate width and  $0.23\text{-}\mu\text{m}$  gate length produced 7.65 W/mm output power at 18 GHz. Further studies are required to directly compare the effectiveness of polyimide to other passivation schemes.

#### ACKNOWLEDGMENT

The authors would like to thank J. Hughes, and W. Hafez for helpful discussions.

#### REFERENCES

- [1] L. F. Eastman, "Experimental power-frequency limits of AlGaIn–GaIn HEMTs," in *IEEE MTT-S Tech. Dig.*, 2002, pp. 2273–2275.
- [2] J. R. Shealy, V. Kaper, V. Tilak, T. Prunty, J. A. Smart, B. Green, and L. F. Eastman, "An AlGaIn–GaIn high-electron mobility transistor with an AlN sub-buffer layer," *Phys. Rev. B, Condens. Matter*, vol. 14, pp. 3499–3505, 2002.
- [3] Y. Ando, Y. Okamoto, H. Miyamoto, T. Nakayama, T. Inoue, and M. Kuzuhara, "10-W/mm AlGaIn–GaIn HFET with a field modulating plate," *IEEE Electron Device Lett.*, vol. 24, pp. 289–291, Mar. 2003.
- [4] W. L. Pribble, J. W. Palmour, S. T. Sheppard, R. P. Smith, S. T. Allen, T. J. Smith, Z. Ring, J. J. Sumakeris, A. W. Saxler, and J. W. Milligan, "Applications of SiC MESFETs and GaIn HEMTs in power amplifier design," in *IEEE MTT-S Tech. Dig.*, vol. 3, 2002, pp. 1819–1822.
- [5] H. Kim, R. M. Thompson, V. Tilak, T. R. Prunty, J. R. Shealy, and L. F. Eastman, "Effects of SiN passivation and high-electric field on AlGaIn–GaIn HFET degradation," *IEEE Electron Device Lett.*, vol. 24, pp. 421–423, July 2003.
- [6] M. M. Wong, U. Chowdhury, D. Sicault, D. T. Becher, J. C. Denyszyn, J. H. Choi, T. G. Zhu, M. Feng, and R. D. Dupuis, "Improved performance of AlGaIn–GaIn heterojunction field-effect transistors using delta doping and a binary barrier," *Jpn. J. Appl. Phys.*, vol. 42, pp. L353–L355, 2003.
- [7] J. C. Coburn, M. T. Pottiger, S. C. Noe, and S. D. Senturia, "Stress in polyimide coatings," *J. Polym. Sci. B, Polym. Phys.*, vol. 32, no. 7, pp. 1271–1283, 1994.
- [8] C. Goldsmith, P. Geldermans, F. Bedetti, and G. A. Walker, "Measurement of stresses generated in cured polyimide films," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 2, no. 1, pp. 407–409, 1983.
- [9] H. W. Van Zeijl and L. K. Nanver, "Characterization of low-stress LPCVD silicon nitride in high frequency BJTs with self-aligned metallization," in *Proc. Int. Conf. Solid-State and Integrated Circuit Technology*, 1998, pp. 98–101.